AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended): A semiconductor memory device, comprising:

a cell area having N+1 number of unit cell blocks, each including M number of word lines wherein the N number of unit cell blocks are each corresponded to a logical cell block address and one unit cell block is added for accessing data with high speed;

a predetermined cell block table for storing candidate information representing at least more than one candidate word line among the M * (N+1) number of the word lines; and

a tag block for receiving a row address, sensing the logical cell block address in ~~the~~ an inputted row address and outputting a physical cell block address based on the logical cell block address and the candidate information,

wherein the tag block includes:

N+1 number of unit tag tables corresponding to the N+1 number of unit cell blocks, each having M number of registers, the M number of registers corresponding to M number of word lines of corresponding unit cell blocks, each register storing one logical cell block address ~~in~~; and

an initialization unit for initializing the N+1 number of unit tag tables.

Claim 2 (Previously Presented): The semiconductor memory device as recited in claim 1, further comprising:

a control means for controlling the tag block and the predetermined cell block table for activating one word line of a unit cell block selected by the physical cell block address.

Claim 3 (Currently Amended): The semiconductor memory device as recited in claim 1, wherein the initialization unit includes:

a plurality of logical OR gates respectively corresponding to the N+1 number of unit cell blocks for respectively receiving an initialization enable signal to enable the N+1 number of unit tag tables and a tag table selection signal to select one of the N+1 number of unit tag tables and respectively outputting a corresponding initialization activating signals to the corresponding unit tag tables;

a plurality of first multiplexers controlled by the initialization ~~selection~~enable signal and respectively corresponding to the N+1 number of unit cell blocks for ~~selectively~~ outputting ~~one of~~either the logical cell block address ~~and~~or an initialization signal ~~to initialize~~ initializing corresponding unit tag tables of the N+1 number of unit tag tables; and

a plurality of second multiplexers controlled by the initialization ~~selection~~ enable signal and respectively corresponding to the N+1 number of unit cell blocks for selectively outputting one of ~~a~~ plural local addresses to select one of M number of word lines of corresponding unit cell blocks and an initialization address to select all registers included in the corresponding unit tag table.

Claim 4 (Currently Amended): A method for controlling a tag block ~~for assigning a physical unit cell address based on a logical unit cell block~~, comprising:

initializing the tag block in a semiconductor memory device; and

performing a data access operation of the semiconductor memory device in response to a physical unit cell address outputted from ~~by using~~ the tag block sensing a logical cell block address,

wherein the initializing the tag block in a semiconductor memory device including:

nullifying ~~a~~ N+1 number of unit tag tables of the tag block;

selecting all of the N+1 number of unit tag tables; and

storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Claim 5 (Canceled)

Claim 6 (Currently Amended): A method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a tag block having N+1 number of unit tag tables~~blocks~~ for sensing a logical cell block address to output a physical unit cell address, each having M number of registers for sensing an update of

data, comprising:

nullifying the N+1 number of unit tag tables;

selecting all the N+1 number of unit tag tables; and

storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables,

wherein the N number of unit cell blocks are corresponded to an address and one unit cell block is added for accessing data with high speed.